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Serial Number: 09/737218   Dkt: 703.070US2
Filing Date: December 14, 2000
Title: SYSTEM AND METHOD FOR ASSIGNING ADDRESSES TO MEMORY DEVICES

REMARKS

This responds to the Office Action mailed on February 9, 2004.

Claims 1, 64, 58, and 71 are amended, no claims are canceled, and claim 74 is added; as a result, claims 1-3 and 64-74 are now pending in this application.

Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 Form, listing all references that were submitted with the Information Disclosure Statement filed on December 14, 2000, marked as being considered and initialed by the Examiner, be returned with the next official communication.

§103 Rejection of the Claims

Claims 1-3 and 64-73 were rejected under 35 USC § 103(a) as being unpatentable over Yamada et al. (U.S. 5,617,537).

The rejection stated that Yamada shows, "a plurality of memory devices (21, e.g. 21-1, 21-2 and 21-3) associated with one processor." The rejection further stated that, "each of the memory devices 21-1, 21-2 and 21-3 is associated with any one of the processors 19-1, 19-2, and 19-3 and any one processor may access all of these memory deices via processor interconnect 25."

Yamada appear to show a plurality of memory devices 21-1, 21-2 and 21-3. Yamada also appears to show a plurality of processors 19-1, 19-2, 19-3. However, Applicant is unable to find in Yamada, a plurality of memory devices associated with only one processor, wherein each memory device includes a local address storage circuitry which stores a local address for identifying the storage circuitry's single associated memory device once an address assign command is decoded by a command decoder.

In contrast, claim 1 as amended includes a plurality of memory devices associated with only one processor, wherein each memory device includes a local address storage circuitry which stores a local address for identifying the storage circuitry's single associated memory device once an address assign command is decoded by a command decoder. Further in contrast, claims

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64, 68, and 71 as amended include a processor, and a plurality of memory devices associated with only the processor.

Because Yamada does not show or make obvious every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection are respectfully requested with respect to amended claims 1, 64, 68, and 71. Additionally, reconsideration and withdrawal of the rejection are respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

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CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,
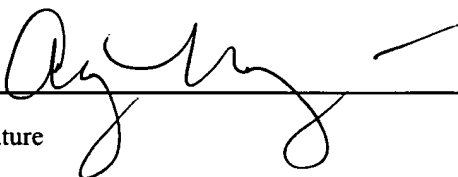
ROBERT D. NORMAN

By his Representatives,

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Date ____4- 8-0 4____   By _____

David C. Peterson
Reg. No. 47,857

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this __8th__ day of April, 2004.

____Amy Moriarty____   _____

Name   Signature